

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It combines one N Channel MOSFET and one P channel MOSFET.

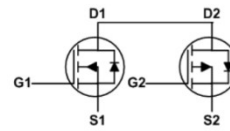
• Features

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Dual DIE in one package

• Application

- Power Management in Notebook Computer
- BLDC Motor driver

• Product Summary



$V_{DS1} = 60V$
 $V_{DS2} = -60V$
 $R_{DS(ON)1} = 20m\Omega$
 $R_{DS(ON)2} = 23m\Omega$
 $I_{D1} = 25A$
 $I_{D2} = -23A$



TO-252-4

• Ordering Information:

Part NO.	ZMC88606D
Marking	ZMC88606
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2500

• N Channel Absolute Maximum Ratings ($T_c = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D @ T_c = 25^\circ C$	25	A
	$I_D @ T_c = 75^\circ C$	20	A
	$I_D @ T_c = 100^\circ C$	16	A
Pulsed Drain Current ^①	I_{DM}	75	A
Total Power Dissipation	$P_D @ T_c = 25^\circ C$	50	W
Total Power Dissipation	$P_D @ T_A = 25^\circ C$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$
Single Pulse Avalanche Energy	E_{AS}	20	mJ

•P Channel Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	$I_D @ T_C = 25^\circ\text{C}$	-23	A
	$I_D @ T_C = 75^\circ\text{C}$	-18	A
	$I_D @ T_C = 100^\circ\text{C}$	-15	A
Pulsed Drain Current ^①	I_{DM}	-54	A
Total Power Dissipation	$P_D @ T_C = 25^\circ\text{C}$	50	W
Total Power Dissipation	$P_D @ T_A = 25^\circ\text{C}$	2.0	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	35	mJ

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	2.1	$^\circ\text{C/W}$
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	$^\circ\text{C/W}$
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	265	$^\circ\text{C}$

•N Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.3	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 8A$		20	26	m Ω
		$V_{GS} = 4.5V, I_D = 6A$		24	30	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 25V, I_D = 5A$		7		s
Source-drain voltage	V_{SD}	$I_S = 12A$			1.28	V

•N Channel Dynamic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	R _g	f = 1MHz		1.4		Ω
Input capacitance	C _{iss}	f = 1MHz V _{DS} =25V	-	1690	-	pF
Output capacitance	C _{oss}		-	121	-	
Reverse transfer capacitance	C _{rss}		-	91	-	
Total gate charge	Q _g	V _{DD} = 25V I _D = 5A V _{GS} = 10V	-	26	-	nC
Gate - Source charge	Q _{gs}		-	5.9	-	
Gate - Drain charge	Q _{gd}		-	5.9	-	

•P Channel Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250uA	-60			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250uA	-1.2		-2.5	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = -60V, V _{GS} = 0V			-1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} = -10V, I _D = -16A		23	30	mΩ
		V _{GS} = -4.5V, I _D = -12A		45	65	mΩ
Source-drain voltage	V _{SD}	I _S = -12A			-1.28	V
Forward Transconductance	g _{FS}	V _{DS} = -5V, I _D = -5A		1.5		s

•P Channel Dynamic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	R _g	f = 1MHz		7.5		Ω
Input capacitance	C _{iss}	f = 1MHz V _{DS} = -25V	-	3300	-	pF
Output capacitance	C _{oss}		-	148	-	
Reverse transfer capacitance	C _{rss}		-	96	-	
Total gate charge	Q _g	V _{DD} = -25V I _D = -5A V _{GS} = -10V	-	46	-	nC
Gate - Source charge	Q _{gs}		-	6.3	-	
Gate - Drain charge	Q _{gd}		-	8.6	-	

•N Channel characteristics curve

Fig.1 Gate-Charge Characteristics

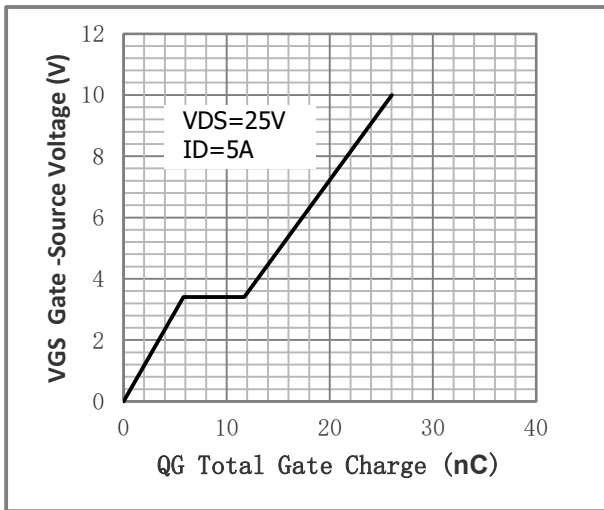


Fig.2 Capacitance Characteristics

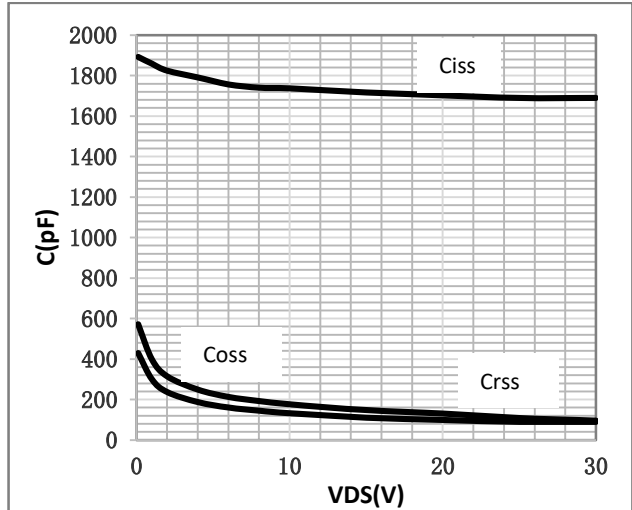


Fig.3 Maximum Continuous Drain Current

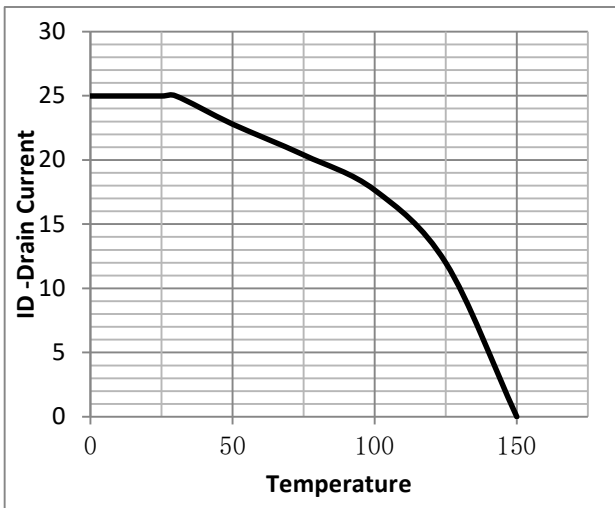


Fig.4 Typical output Characteristics

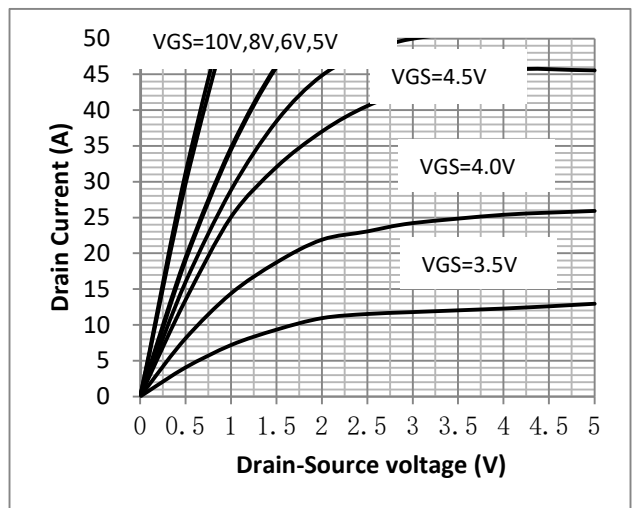


Fig.5 Threshold Voltage V.S Junction Temperature

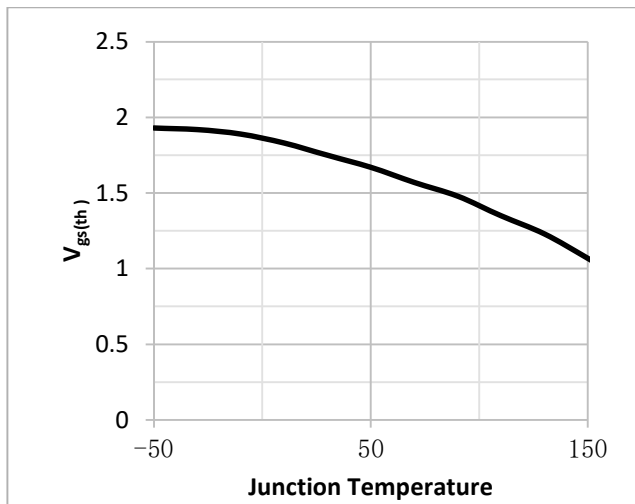


Fig.6 Resistance V.S Drain Current

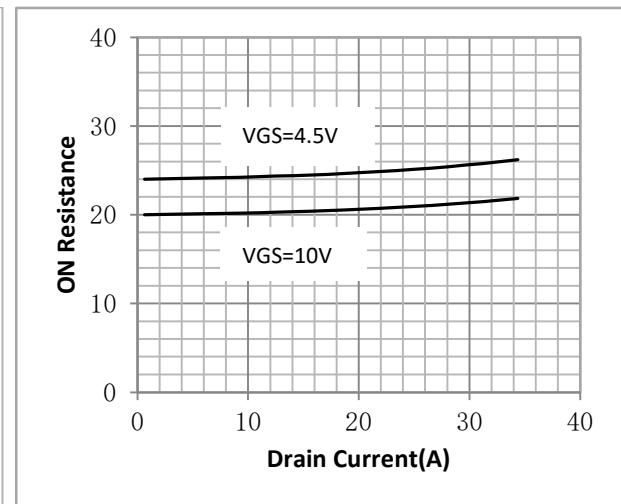


Fig.7 On-Resistance VS Gate Source Voltage

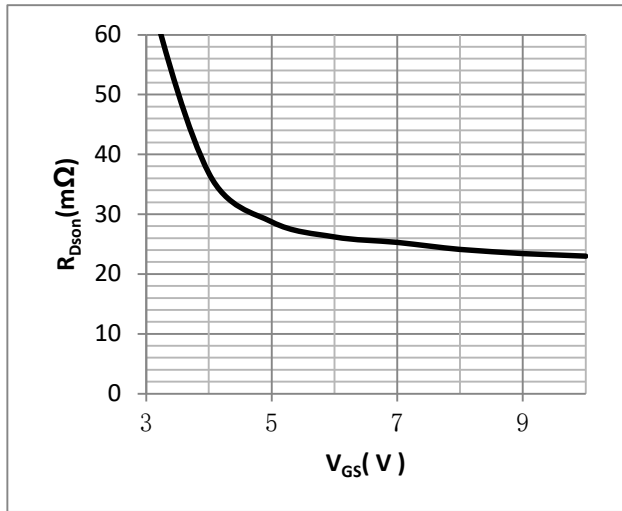


Fig.8 On-Resistance V.S Junction Temperature

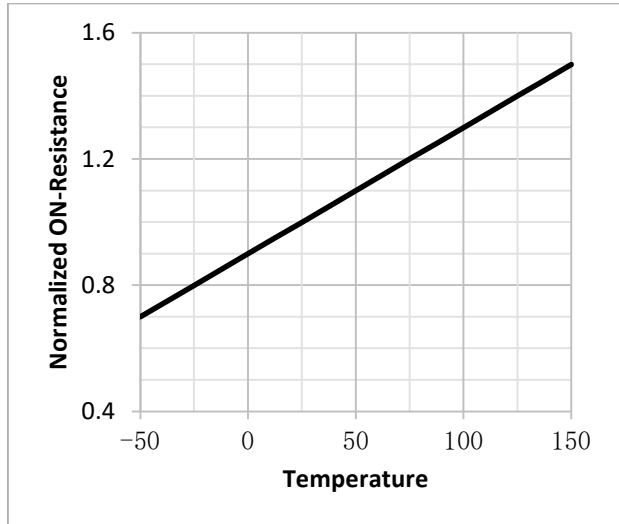


Fig.9 Power Dissipation

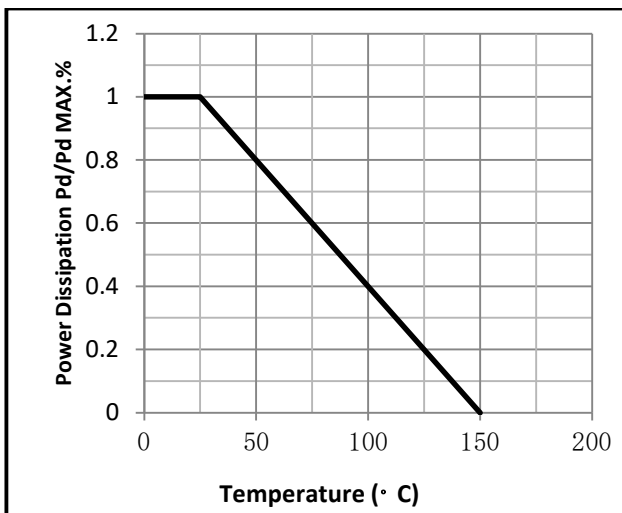


Fig.10 SOA Maximum Safe Operating Area

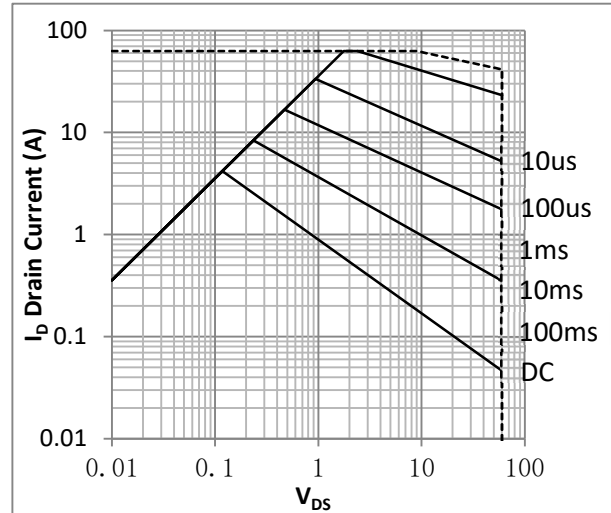


Figure.11 Diode Forward Voltage vs. Current

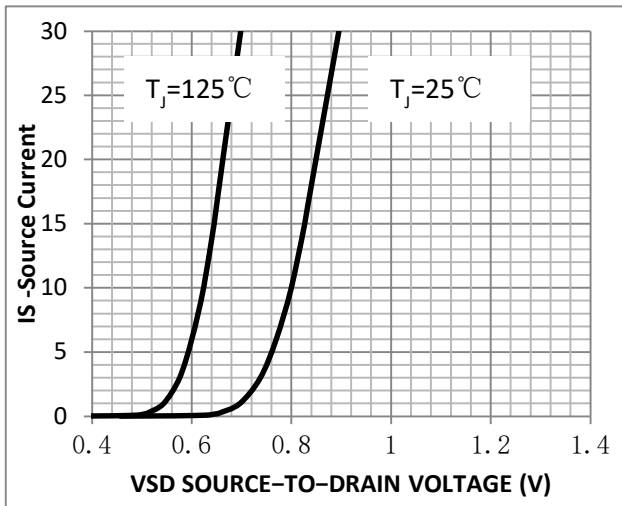
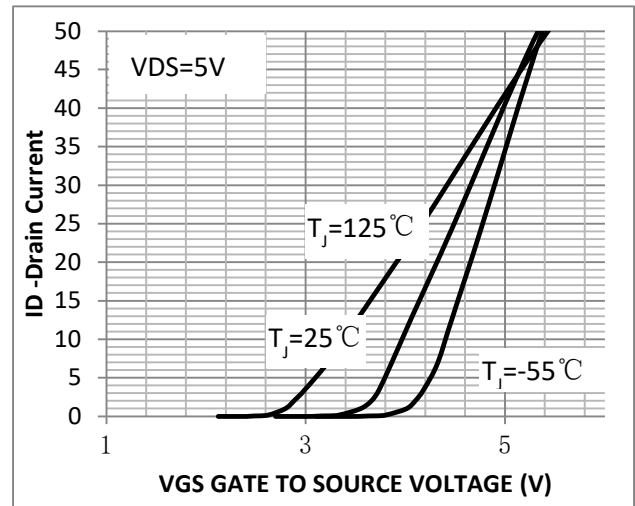


Figure.12 Transfer Characteristics



•P Channel characteristics curve

Fig.1 Gate-Charge Characteristics

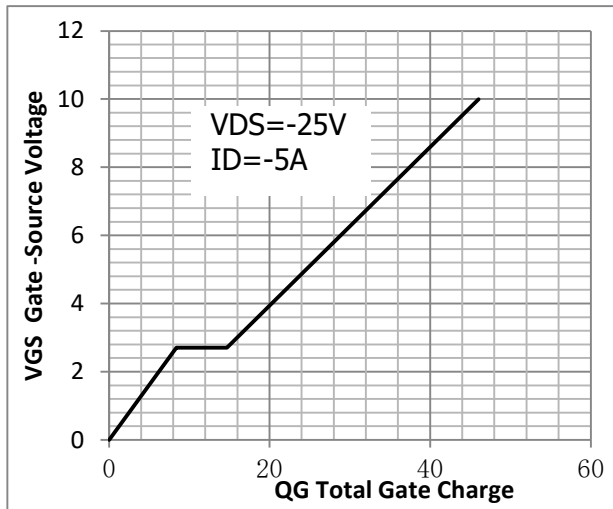


Fig.2 Capacitance Characteristics

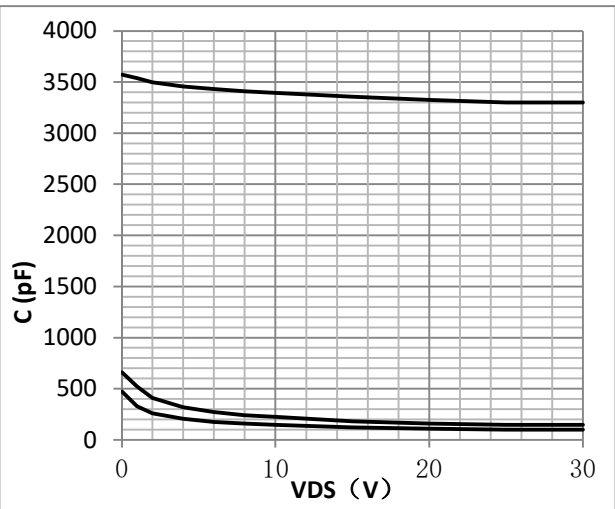


Fig.3 Maximum Continuous Drain Current

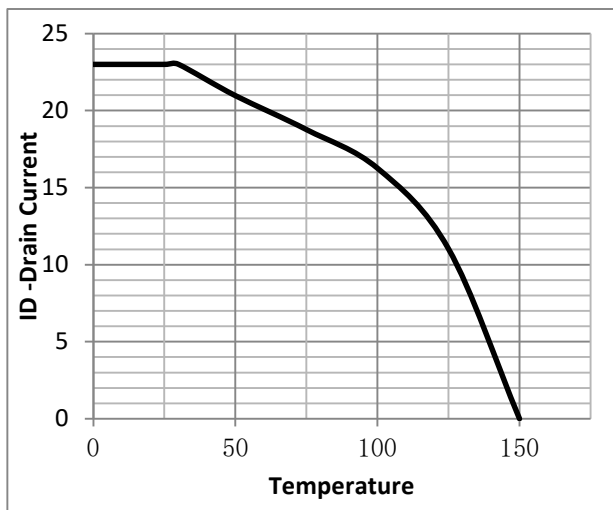


Fig.4 Typical output Characteristics

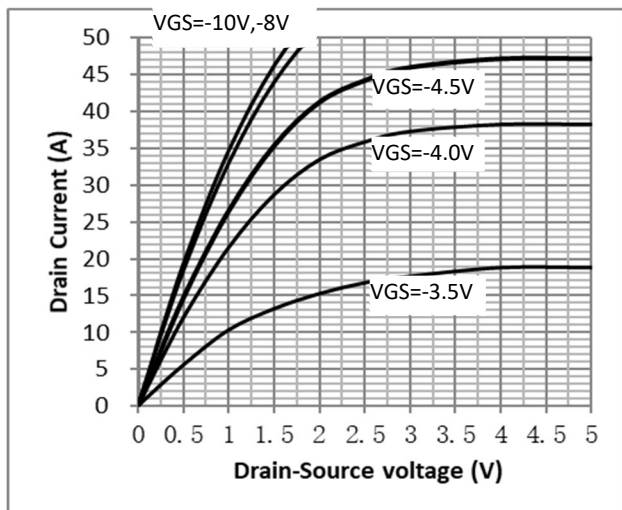


Fig.5 Threshold Voltage V.S Junction Temperature

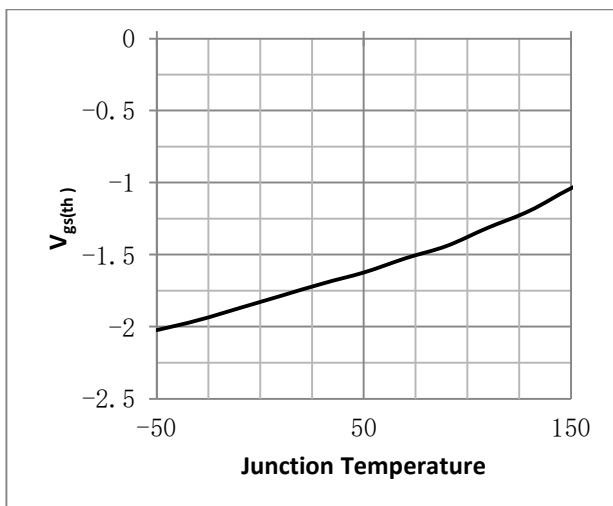


Fig.6 Resistance V.S Drain Current

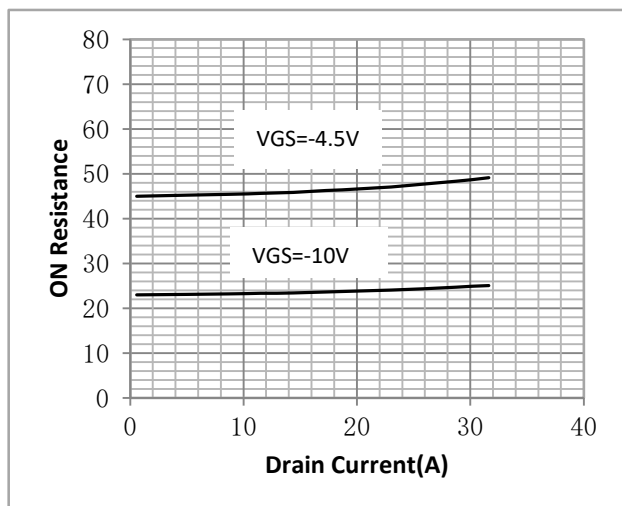


Fig.7 On-Resistance VS Gate Source Voltage

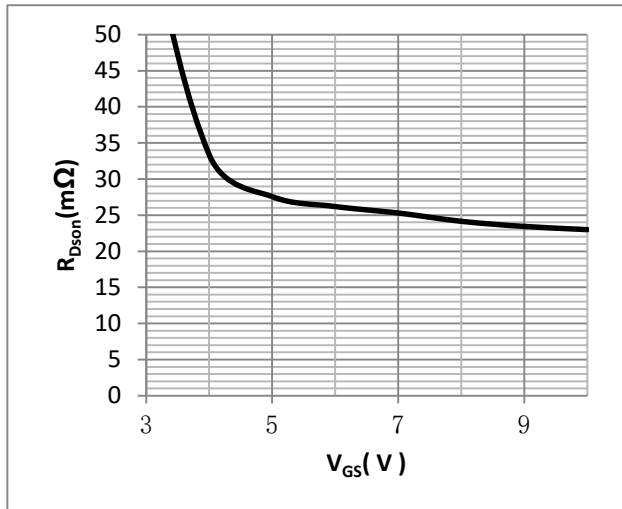


Fig.8 On-Resistance V.S Junction Temperature

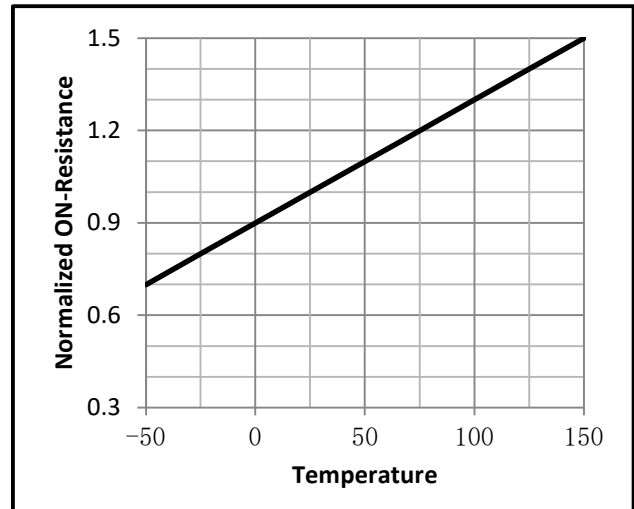


Fig.9 Power Dissipation

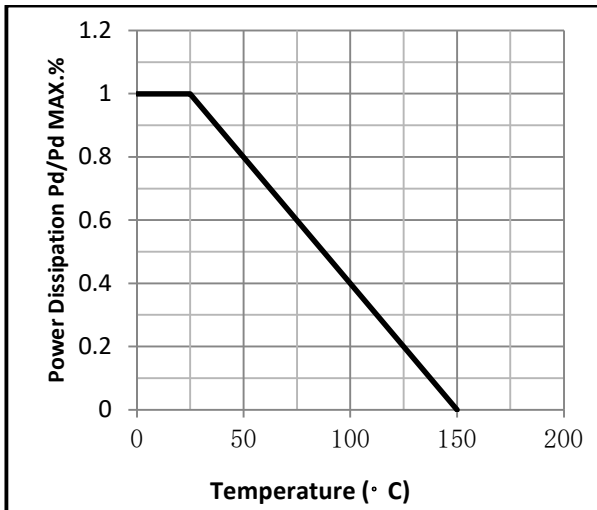


Fig.10 SOA Maximum Safe Operating Area

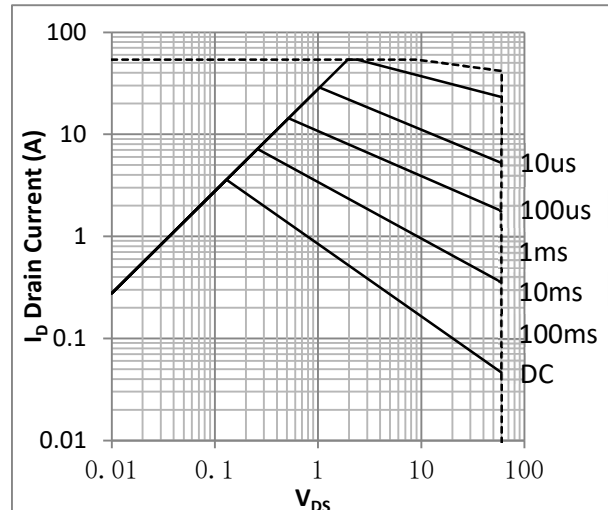


Figure.11 Diode Forward Voltage vs. Current

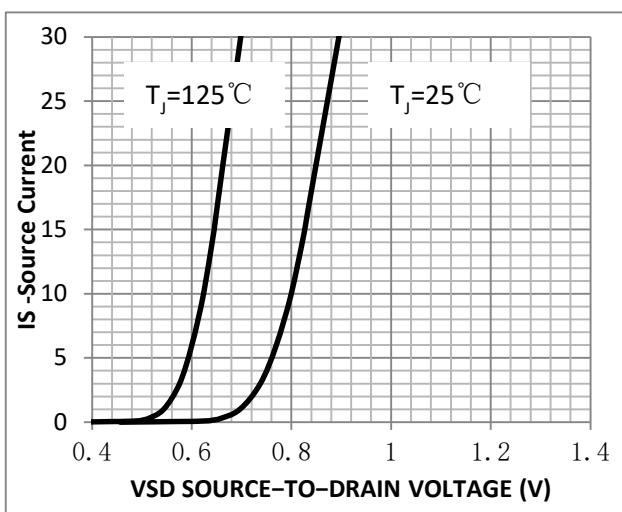
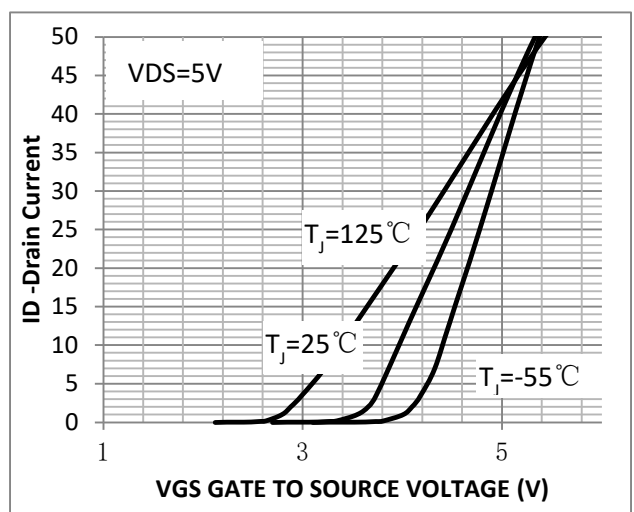


Figure.12 Transfer Characteristics



•Test Circuit

Fig.1 Gate Charge Measurement Circuit

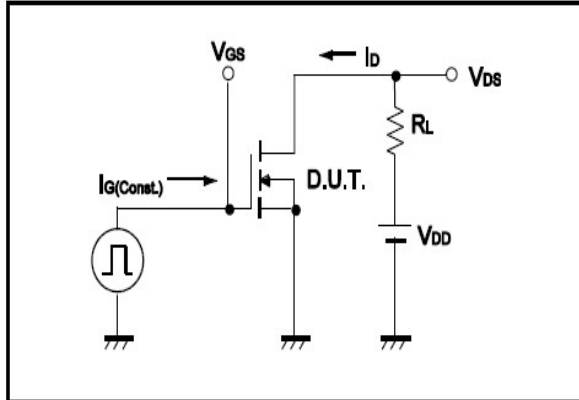


Fig.2 Gate Charge Waveform

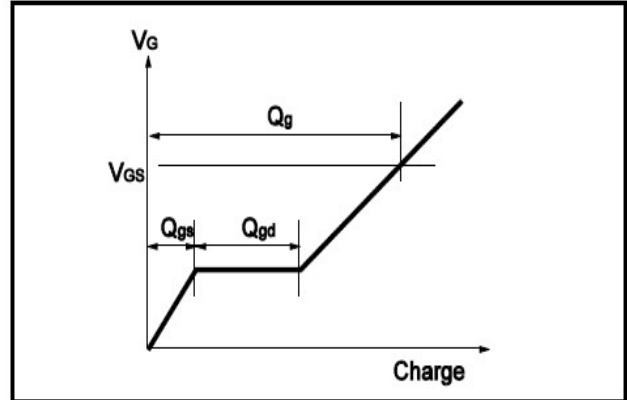


Fig.3 Switching Time Measurement Circuit

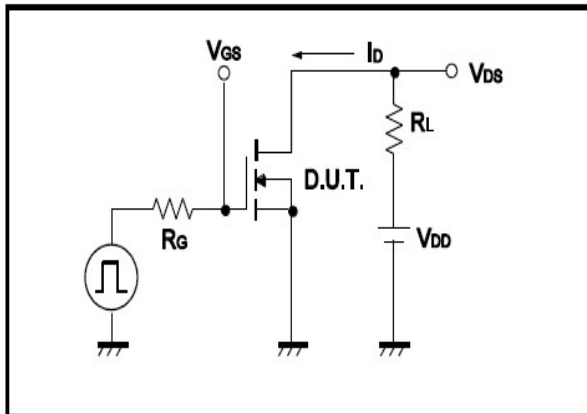


Fig.4 Switching Time Waveform

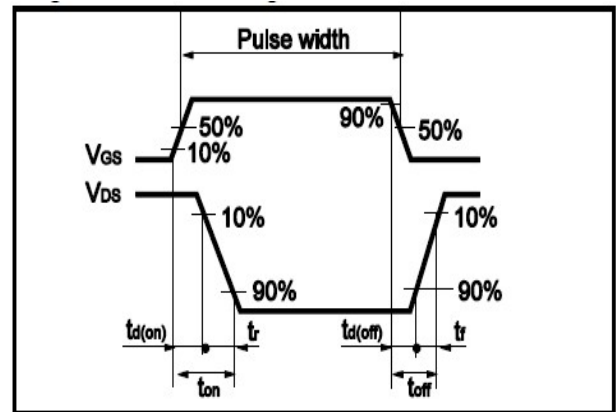


Fig.5 Avalanche Measurement Circuit

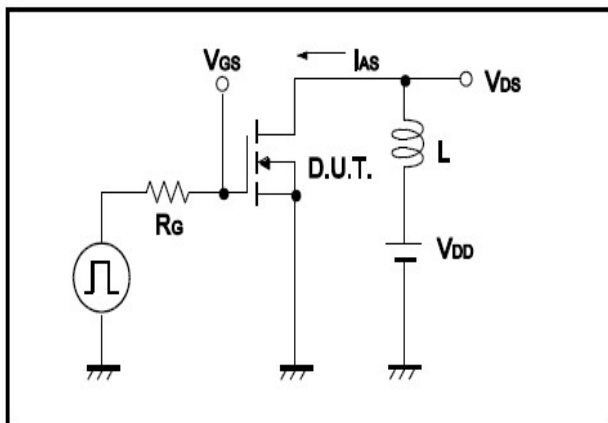
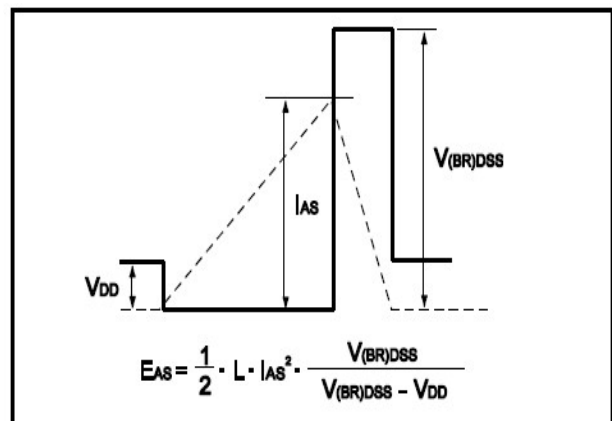


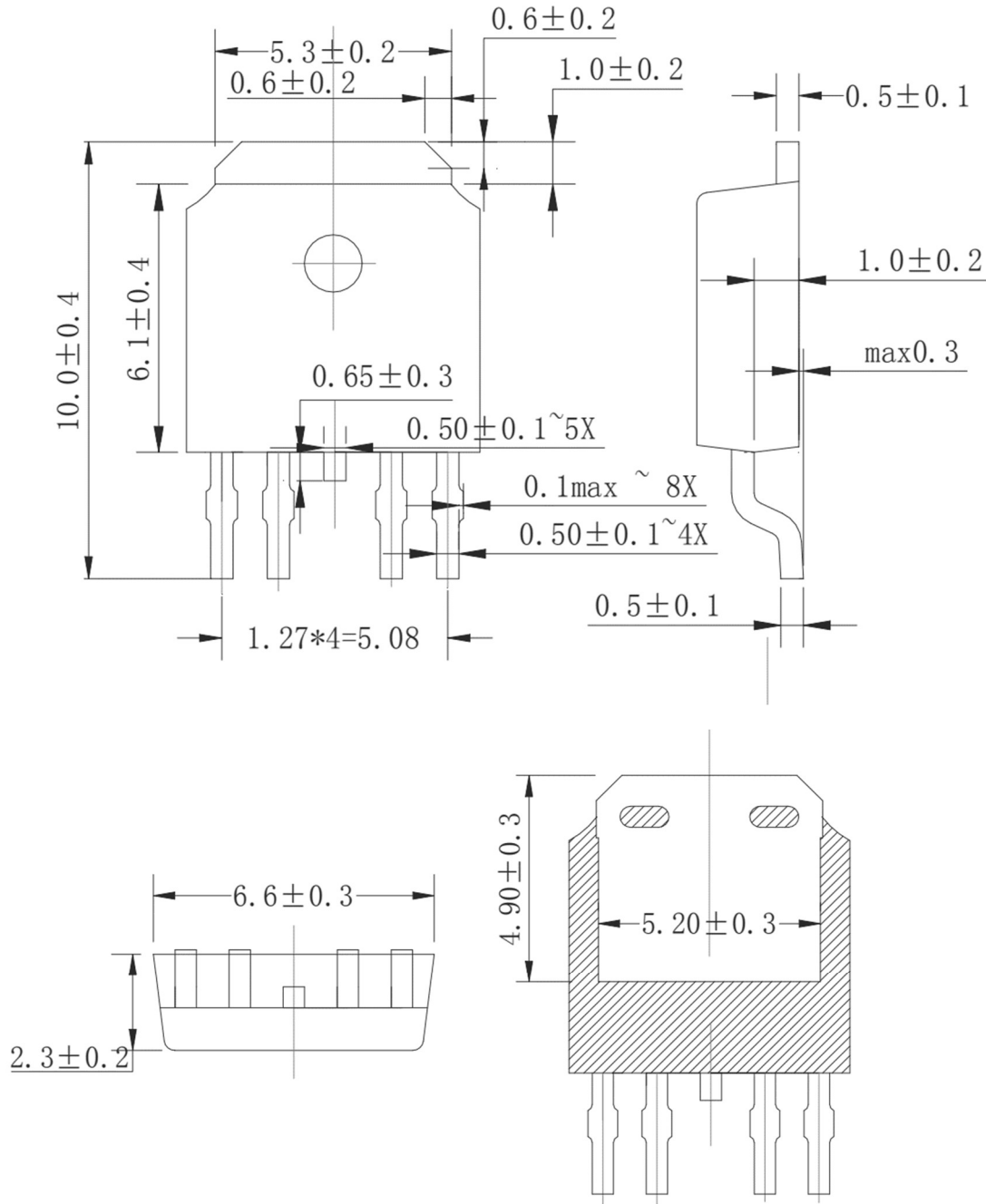
Fig.6 Avalanche Waveform





●Dimensions (TO-252-4)

Unit: mm



Note: ① Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

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